Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-26. (canceled).

27. (previously presented) A method of fabricating a transistor in an integrated circuit device comprising:

providing a semiconductor substrate;

implanting a field implant;

implanting a well implant;

implanting an enhancement implant;

forming a gate oxide on the semiconductor substrate;

forming a gate on the gate oxide;

implanting a first pocket implant into the semiconductor substrate from a first side of the gate; and

implanting a second pocket implant into the semiconductor substrate from a second side of the gate;

diffusing the first pocket implant and the second pocket implant laterally in the semiconductor substrate; and

further doping the first pocket implant and the second pocket implant with a blanket implant,

wherein the first pocket implant and the second pocket implant are in contact at about the center of a channel region.

28. (canceled).

29. (previously presented) The method of claim 27 wherein the first pocket implant and the second pocket implant are implanted at an angle.

30. (previously presented) The method of claim 27 wherein the first pocket implant and the second pocket implant are implanted using the gate as a mask.

31. (previously presented) The method of claim 27 wherein the diffusing increases a reverse short channel effect of the transistor.

32. (canceled).

33. (previously presented) The method of claim 27 further comprising forming a source on the first side of the gate and a drain on the second side of the gate, wherein the source and drain are doped at a first polarity and the first pocket implant and the second pocket implant are doped at a second polarity.

34. (previously presented) The method of claim 33 wherein the first polarity is different than the second polarity.

35. (previously presented) A method of fabricating a transistor in an integrated circuit device comprising:

providing a semiconductor substrate;

forming a gate oxide on the semiconductor substrate;

forming a gate on the gate oxide;

implanting a first pocket implant and a second pocket implant into the semiconductor substrate using the gate as a mask; and

diffusing the first and second pocket implants laterally causing the first pocket implant to merge with the second pocket implant,

wherein the first and second pocket implants are further doped with a blanket implant.

36. (previously presented) The method of claim 35 wherein the diffusing increases a reverse short channel effect of the transistor.

37. (previously presented) The method of claim 35 further comprising implanting an enhancement implant in the semiconductor substrate.

38. (previously presented) A method of fabricating a transistor in an integrated circuit device comprising:

providing a semiconductor substrate having a surface;

forming a gate oxide on the semiconductor substrate surface;

forming a gate on the gate oxide;

implanting a first pocket implant into the semiconductor substrate from a first side of the gate at an angle;

implanting a second pocket implant into the semiconductor substrate from a second side of the gate at an angle; and

diffusing the first and second pocket implants laterally causing the first pocket implant to merge with the second pocket implant,

wherein the first and second pocket implants are further doped with a blanket implant.

39. (canceled).

40. (previously presented) The method of claim 38 wherein the first pocket implant and the second pocket implant are implanted using the gate as a mask.

41. (canceled).

42. (previously presented) A method of fabricating a transistor in an integrated circuit device comprising:

providing a semiconductor substrate having a surface;

forming a gate oxide on the semiconductor substrate surface;

forming a gate on the gate oxide;

implanting a first pocket implant into the semiconductor substrate from a first side of the gate at an angle;

implanting a second pocket implant into the semiconductor substrate from a second side of the gate at an angle; and

diffusing the first and second pocket implants laterally,

wherein the first and second pocket implants are further doped with a blanket implant.

43. (previously presented) The method of claim 42 wherein the diffusing increases a threshold voltage of the transistor.

44. (previously presented) The method of claim 42 further comprising implanting an enhancement implant in the semiconductor substrate.

45-47. (canceled).

48. (previously presented) The method of claim 42 wherein the blanket implant comprises boron.

49. (previously presented) The method of claim 27 wherein the blanket implant comprises boron.

50. (previously presented) The method of claim 49 wherein a dosage of the blanket implant is about 10^{11} cm^{-2}.

51. (previously presented) The method of claim 35 wherein the blanket implant comprises boron.

52. (previously presented) The method of claim 38 wherein the blanket implant comprises boron.